FIG. 1

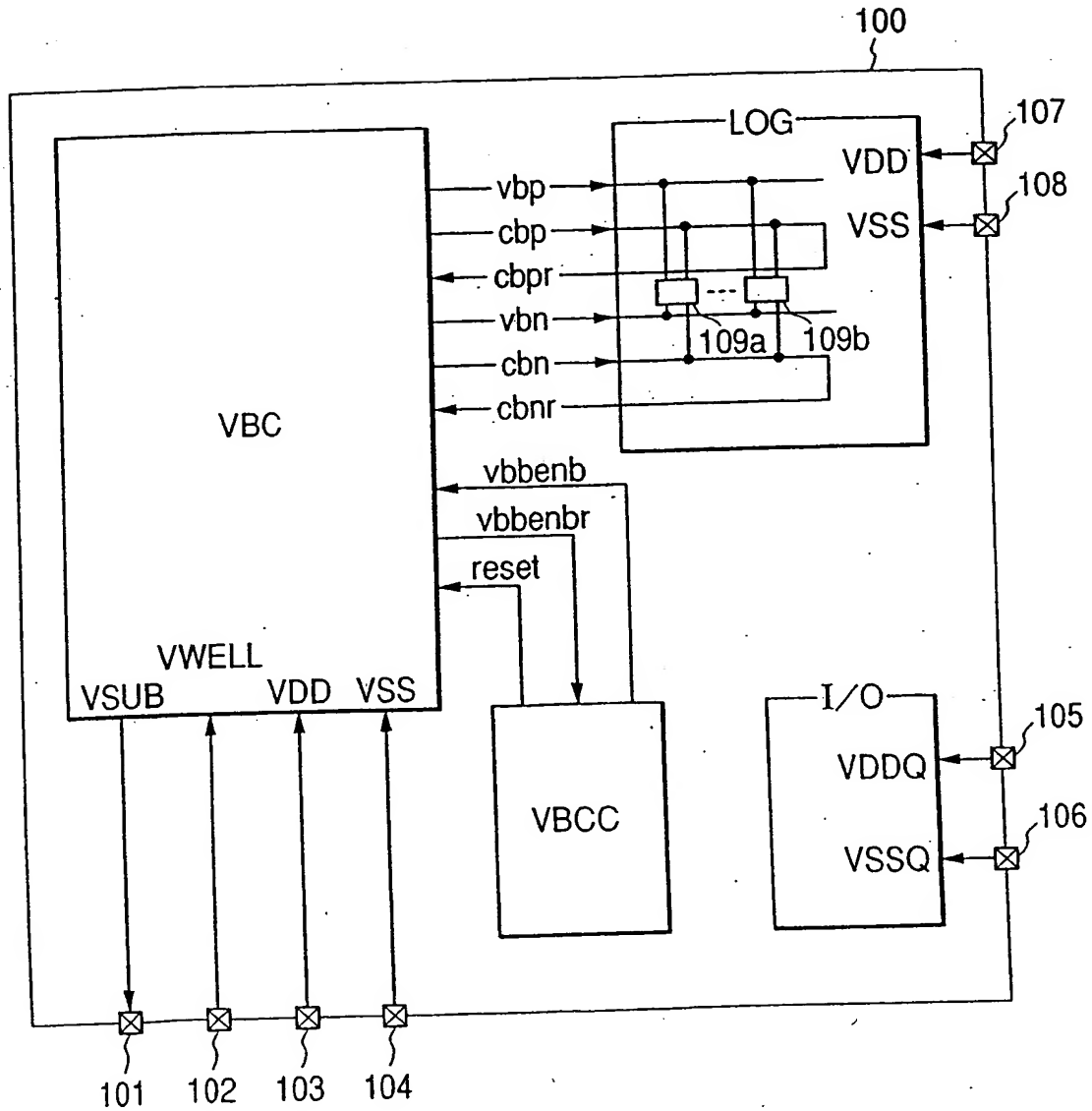

100
LOG
VDD
VSS
107
108
vbp
cbp
cbpr
vbn
cbn
cbnr
109a
109b
VBC
vbbenb
vbbenbr
reset
VWELL
VSUB
VDD
VSS
VBCC
I/O
VDDQ
VSSQ
105
106
101
102
103
104

FIG. 2

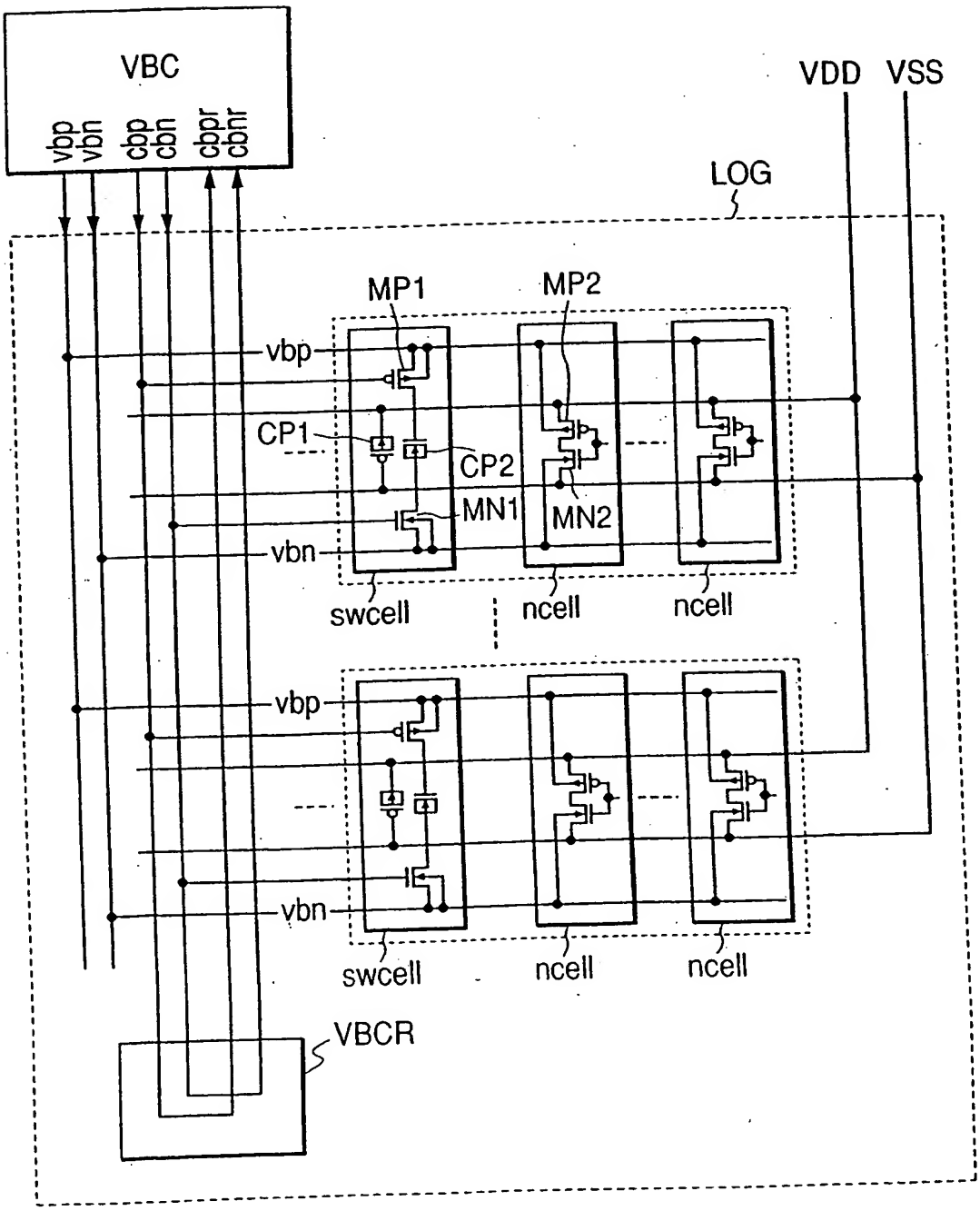
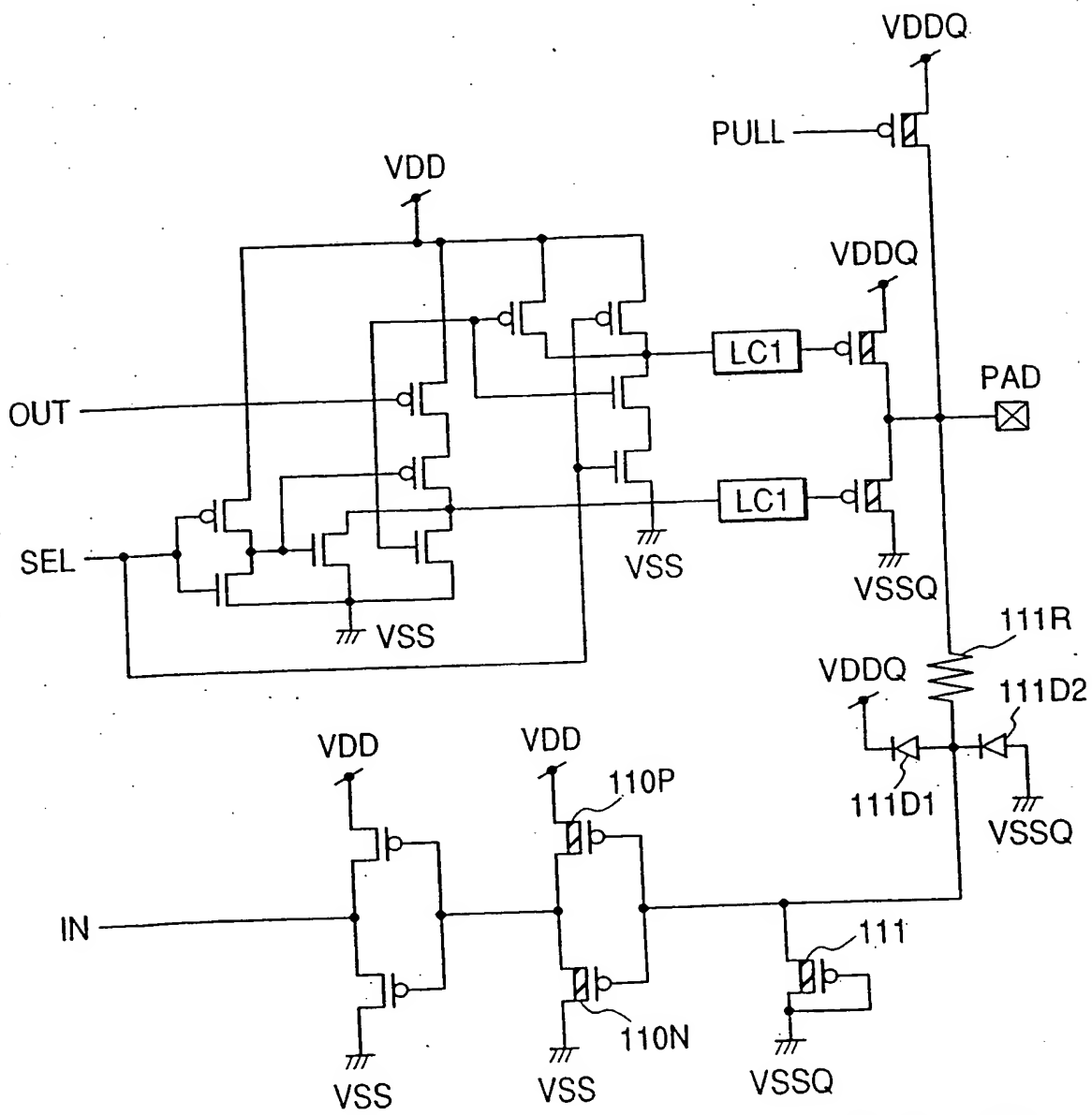

VBC
vbp
vbn
cbp
cbn
cbpr
cbnr
VDD
VSS
LOG
MP1
MP2
vbp
CP1
CP2
MN1
MN2
vbn
swcell
ncell
ncell
vbp
vbn
swcell
ncell
ncell
VBCR

FIG. 3



= THICK OXIDIZATION FILM TRANSISTOR, HIGH THRESHOLD LEVEL, WITHOUT V_{BB} CONTROL

= THIN OXIDIZATION FILM TRANSISTOR, LOW THRESHOLD LEVEL, WITH V_{BB} CONTROL

FIG. 4

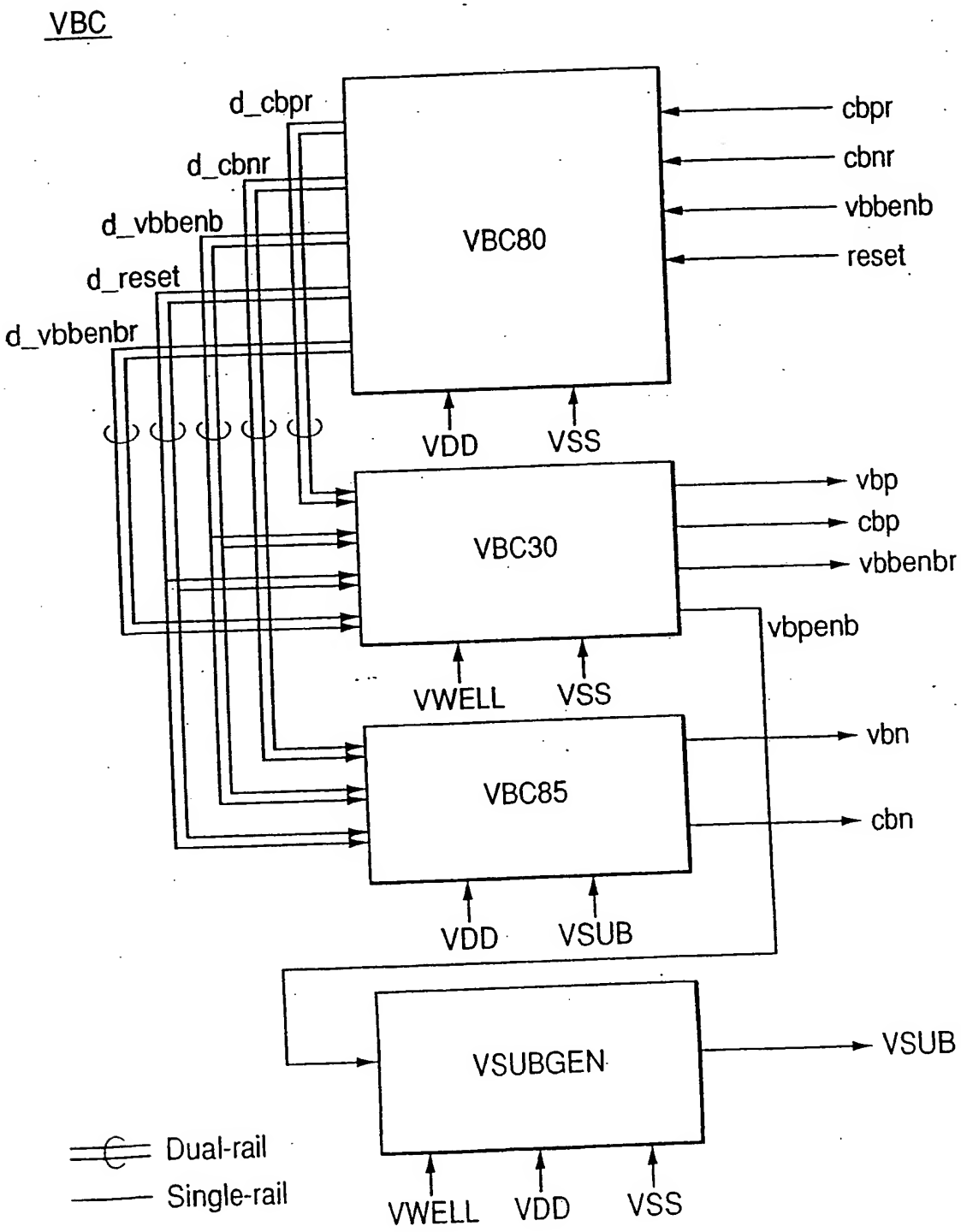

VBC
d_cbpr
d_cbnr
d_vbbenb
d_reset
d_vbbenbr
VBC80
cbpr
cbnr
vbbenb
reset
VDD
VSS
VBC30
vbp
cbp
vbbenbr
vbpenb
VWELL
VSS
VBC85
vbn
cbn
VDD
VSUB
VSUBGEN
VSUB
Dual-rail
Single-rail
VWELL
VDD
VSS

FIG. 5

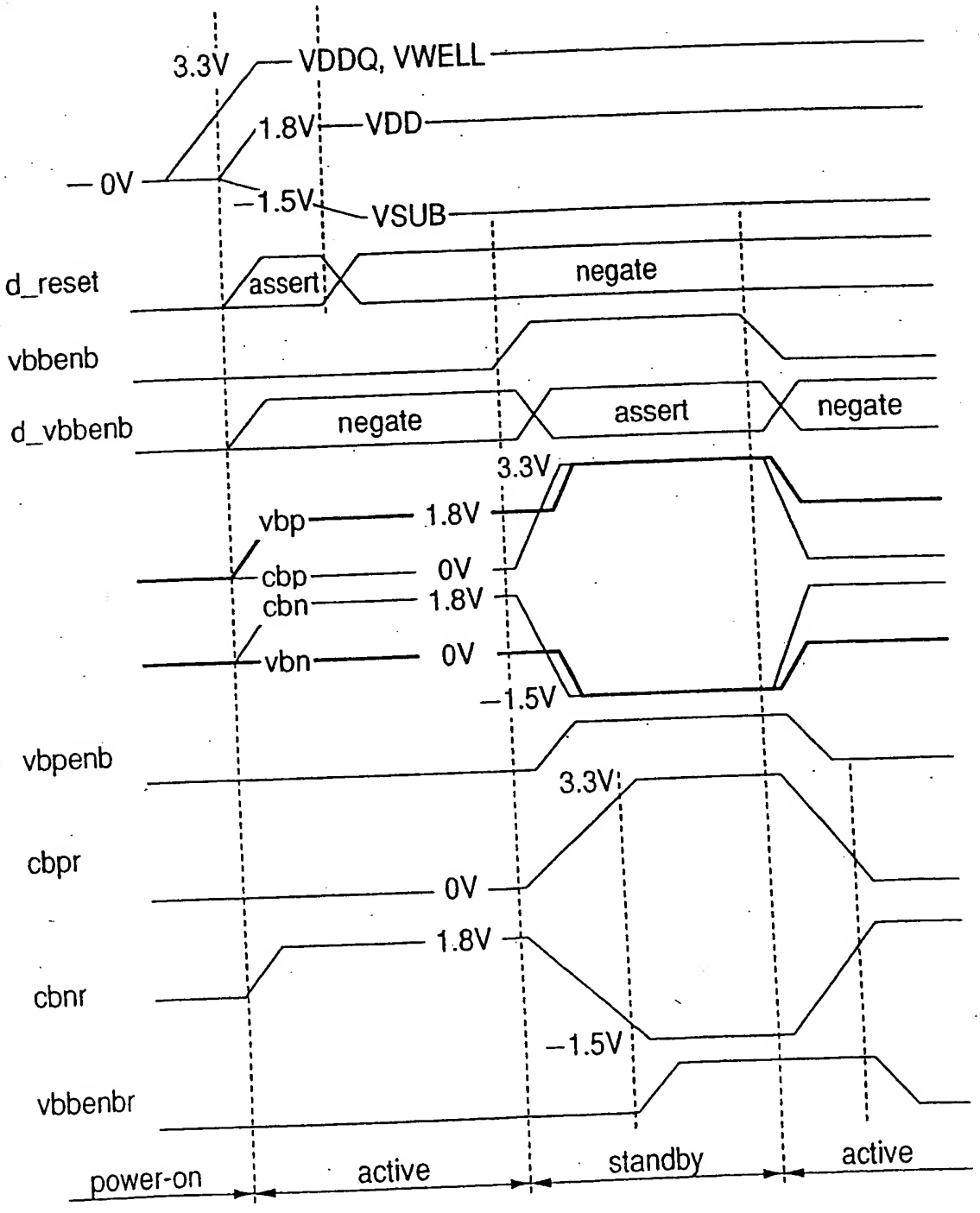

3.3V
VDDQ, VWELL
1.8V
VDD
0V
-1.5V
VSUB
d_reset
assert
negate
vbbenb
d_vbbenb
negate
assert
negate
3.3V
vbp
1.8V
cbp
0V
cbn
1.8V
vbn
0V
-1.5V
vbpenb
3.3V
cbpr
0V
1.8V
cbnr
-1.5V
vbbenbr
power-on
active
standby
active

FIG. 6

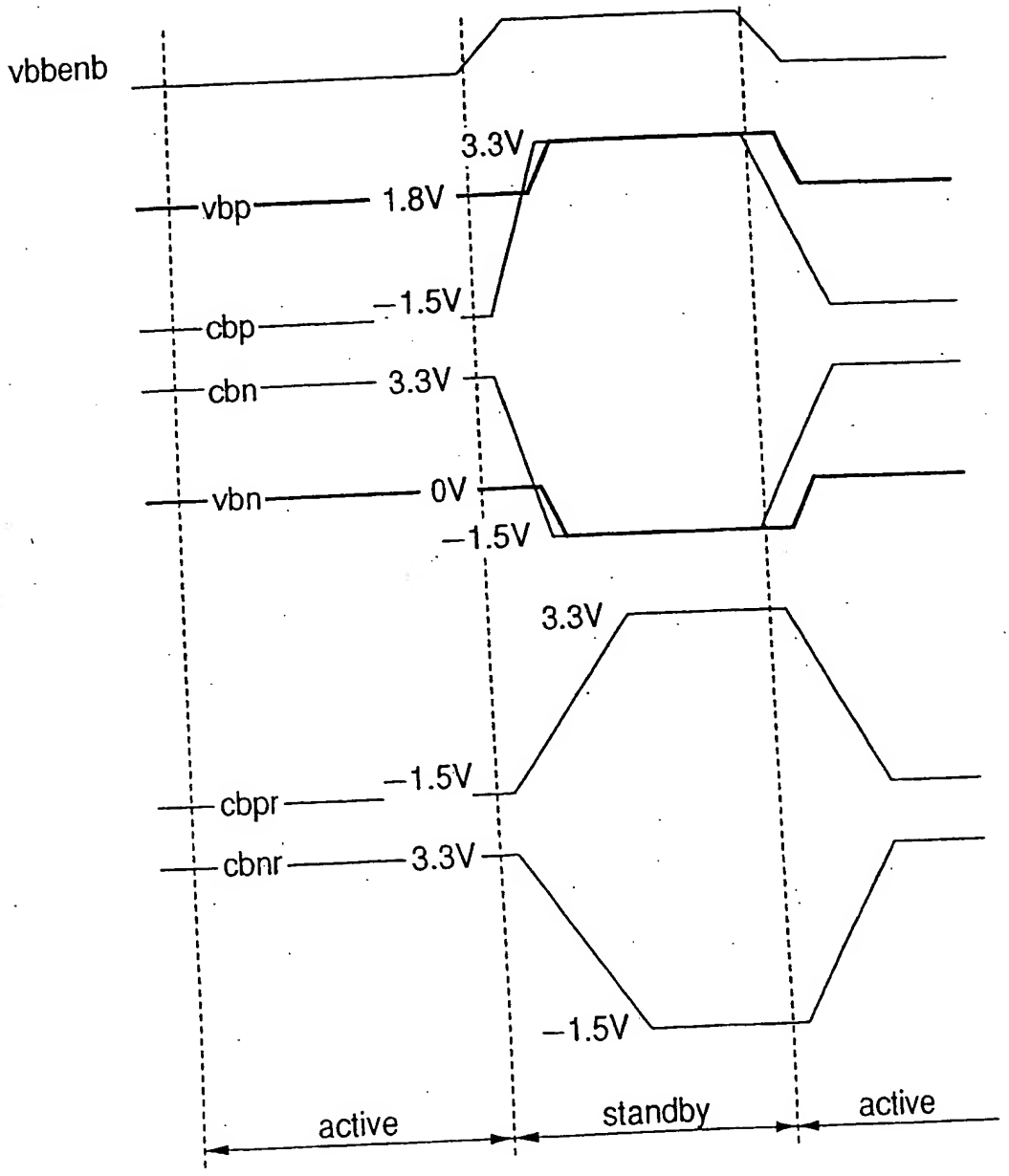

vbbenb
3.3V
vbp
1.8V
cbp
−1.5V
cbn
3.3V
vbn
0V
−1.5V
3.3V
cbpr
−1.5V
cbnr
3.3V
−1.5V
active
standby
active

FIG. 7

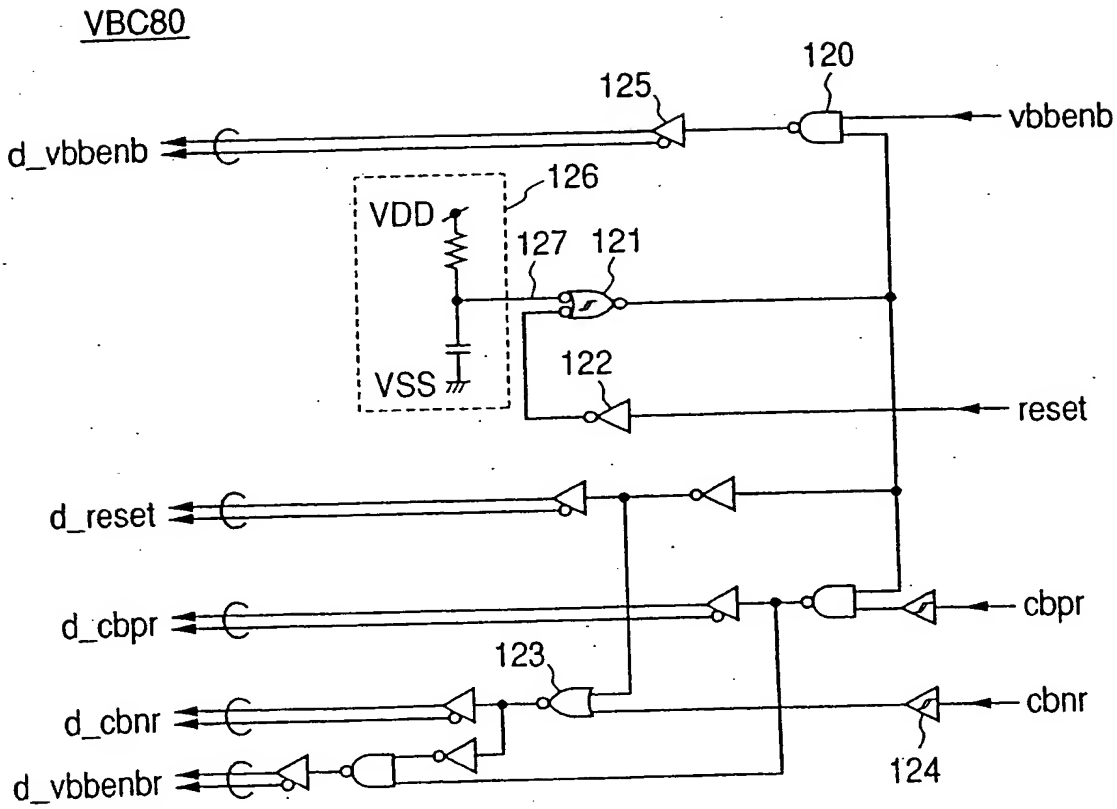

VBC80
120
125
vbbenb
d_vbbenb
126
VDD
127
121
VSS
122
reset
d_reset
d_cbpr
cbpr
123
d_cbnr
cbnr
d_vbbenbr
124

FIG. 8

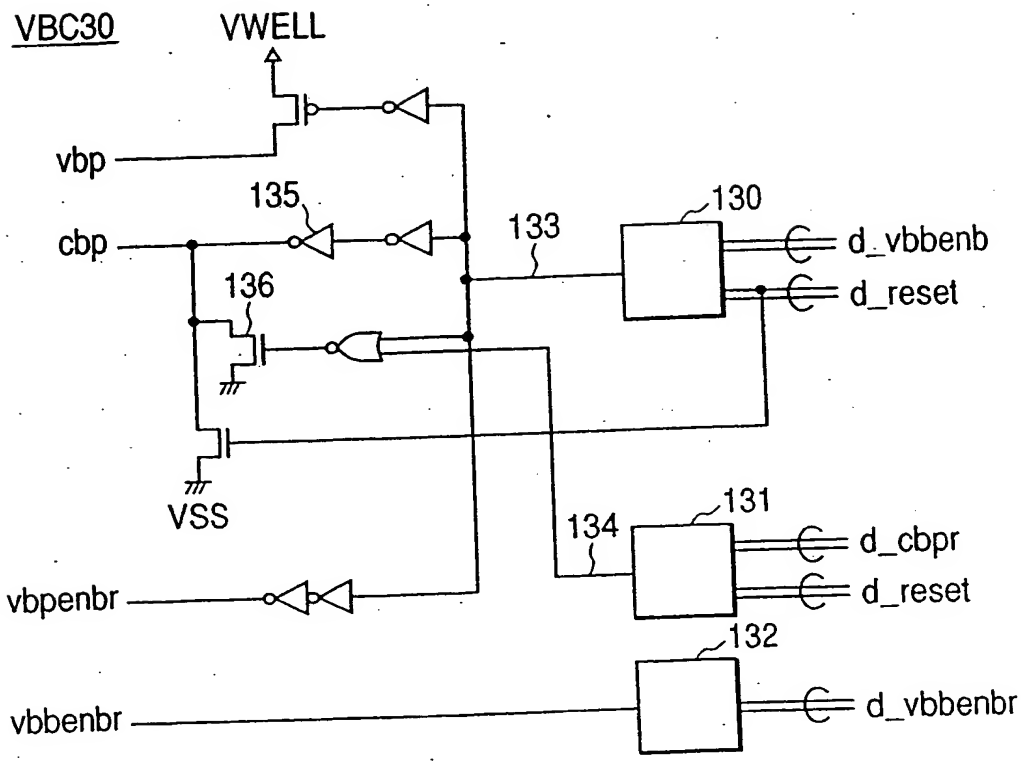

VBC30
VWELL
vbp
cbp
135
133
130
d_vbbenb
d_reset
136
VSS
134
131
d_cbpr
d_reset
vbpenbr
132
vbbenbr
d_vbbenbr

FIG. 9

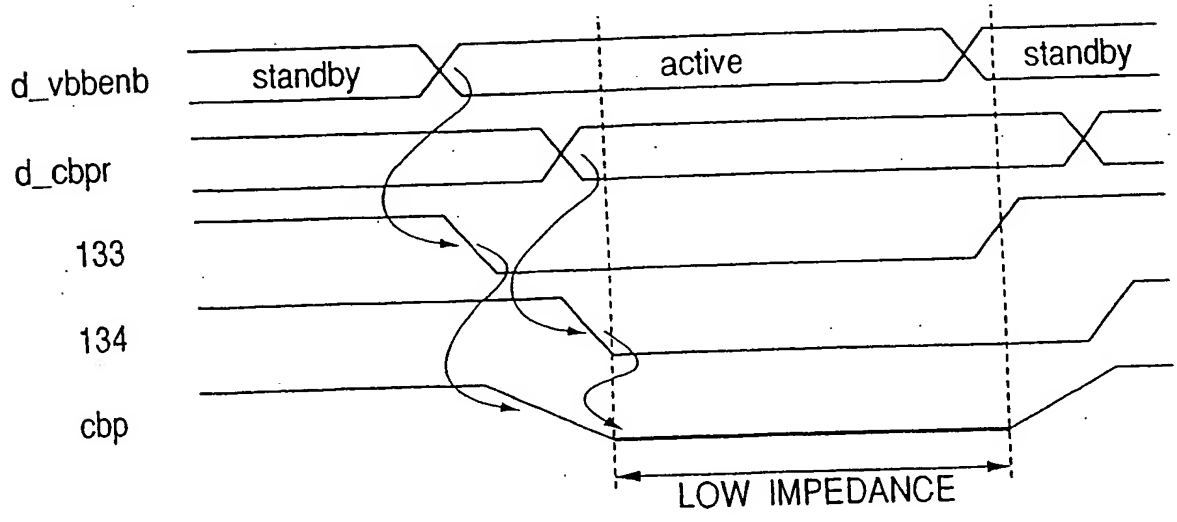

d_vbbenb
standby
active
standby
d_cbpr
133
134
cbp
LOW IMPEDANCE

FIG. 10

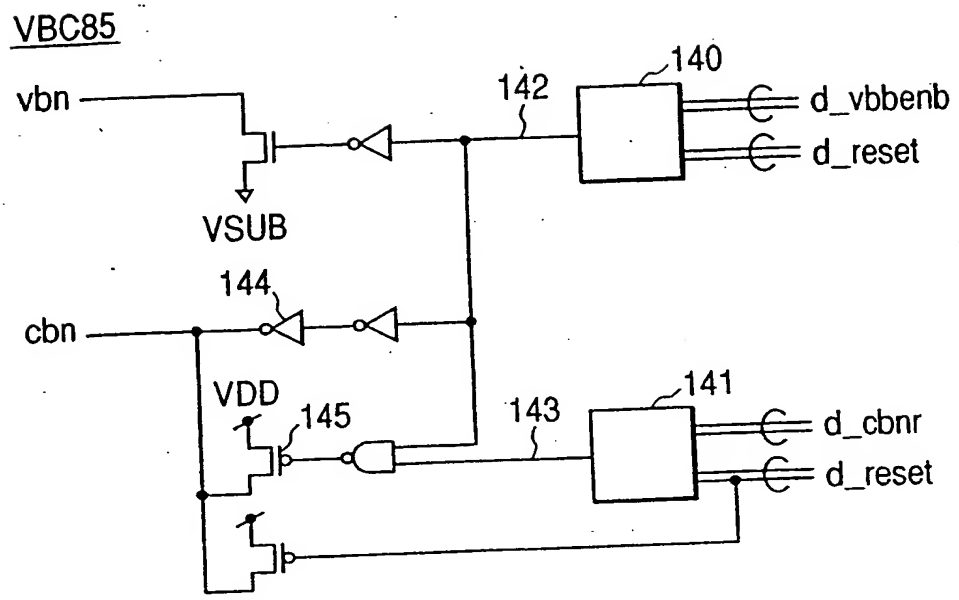

VBC85
vbn
VSUB
142
140
d_vbbenb
d_reset
144
cbn
VDD
145
143
141
d_cbnr
d_reset

FIG. 11

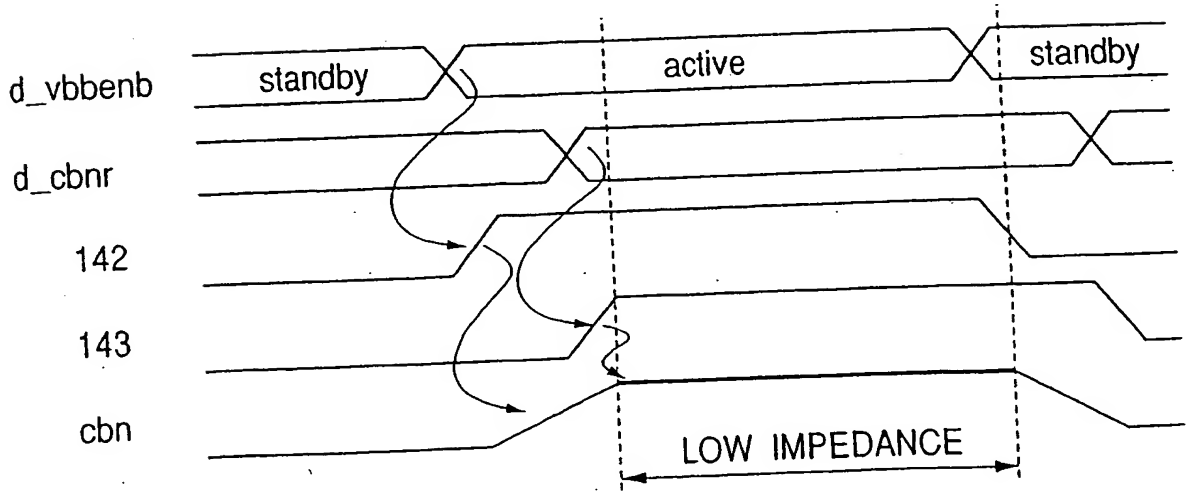

d_vbbenb
d_cbnr
142
143
cbn
standby
active
standby
LOW IMPEDANCE

FIG. 12

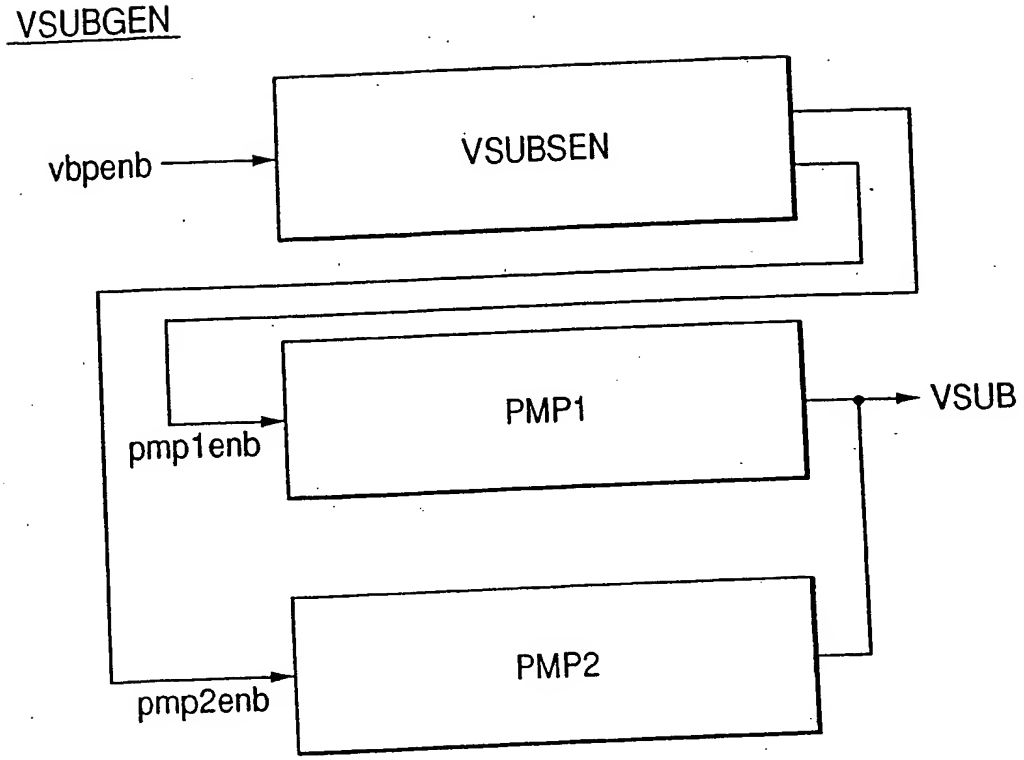

VSUBGEN
vbpenb
VSUBSEN
PMP1
pmp1enb
VSUB
PMP2
pmp2enb

FIG. 13

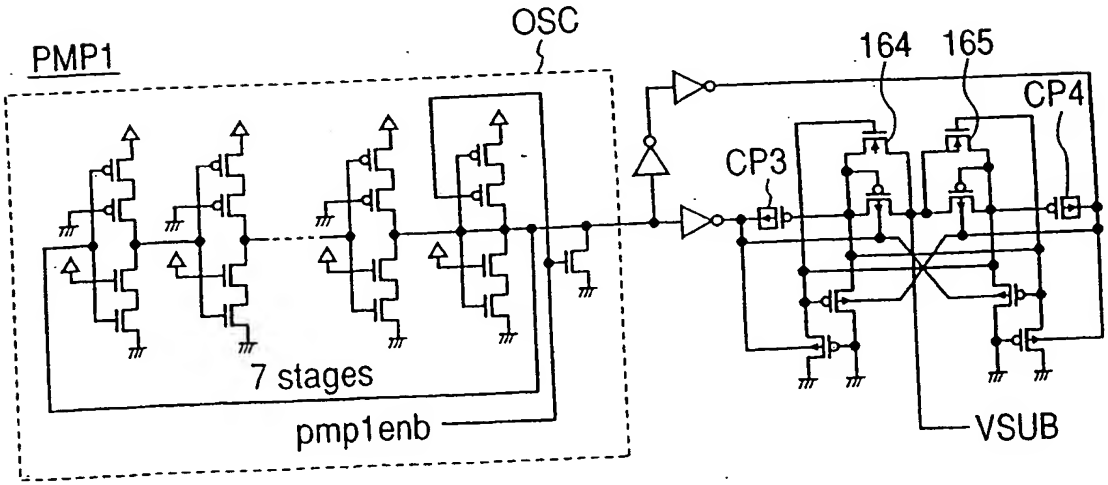

PMP1
OSC
164
165
CP4
CP3
7 stages
pmp1enb
VSUB

FIG. 14

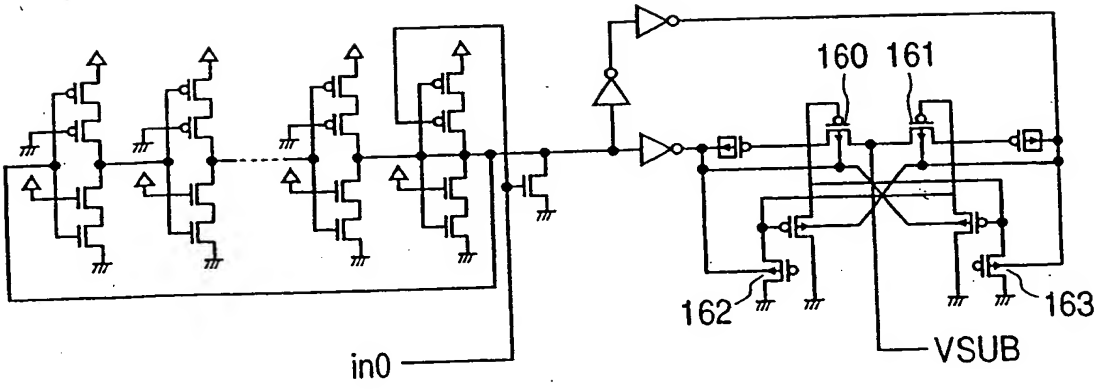


FIG. 15

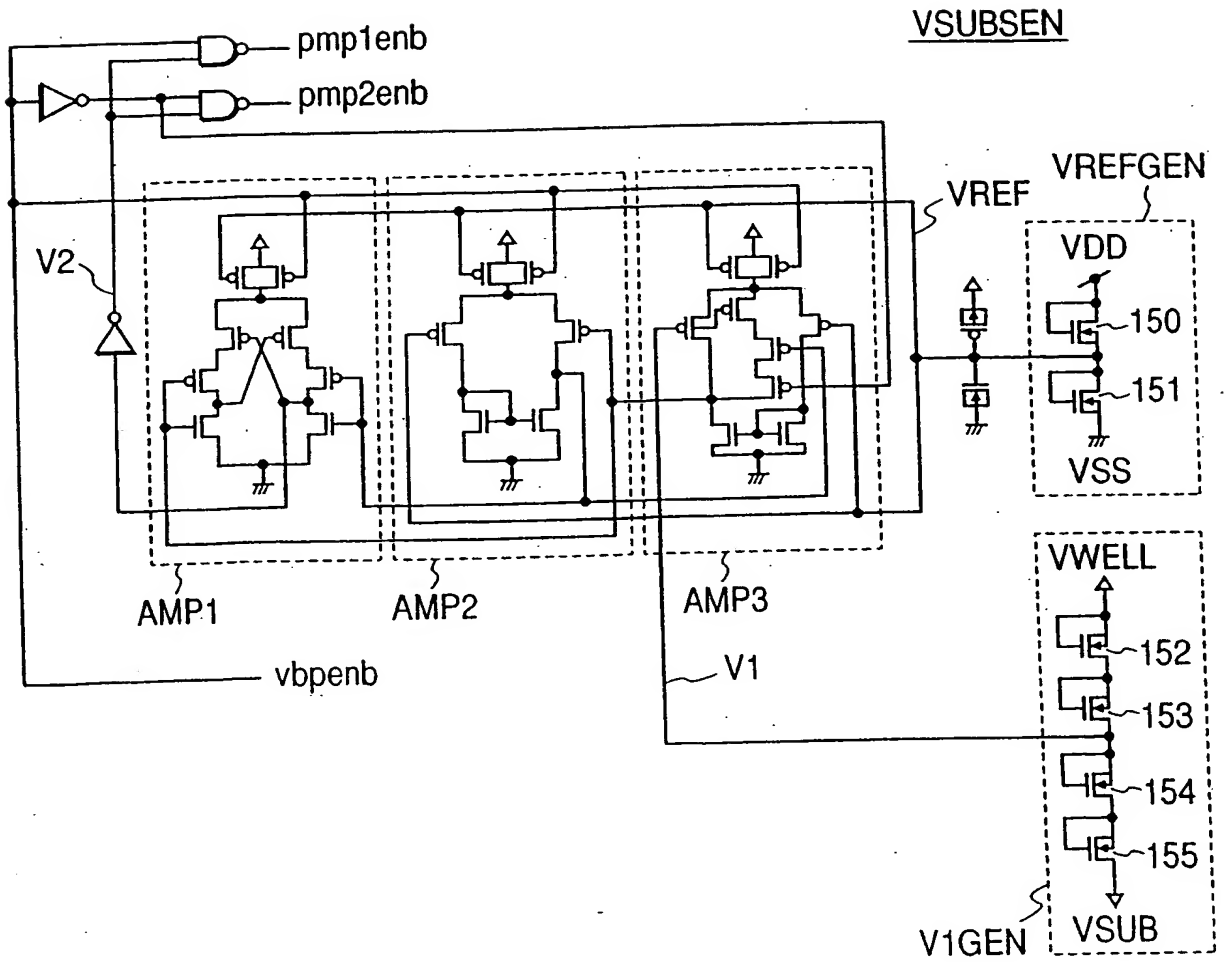

VSUBSEN
pmp1enb
pmp2enb
VREFGEN
VREF
VDD
150
151
VSS
V2
AMP1
AMP2
AMP3
VWELL
152
153
154
155
vbpenb
V1
V1GEN
VSUB

FIG. 16

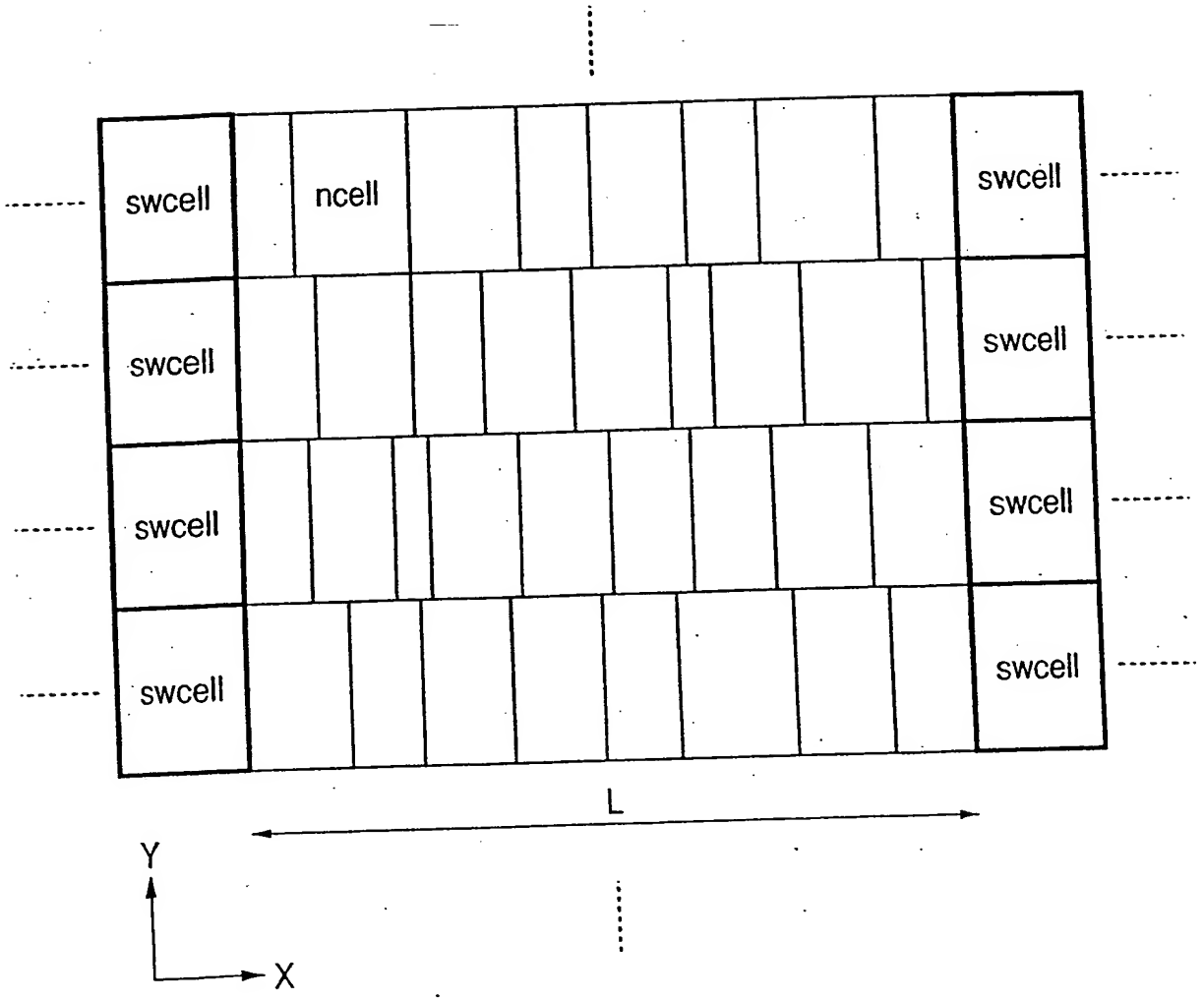

swcell
ncell
swcell
swcell
swcell
swcell
swcell
swcell
swcell
L
Y
X

FIG. 17

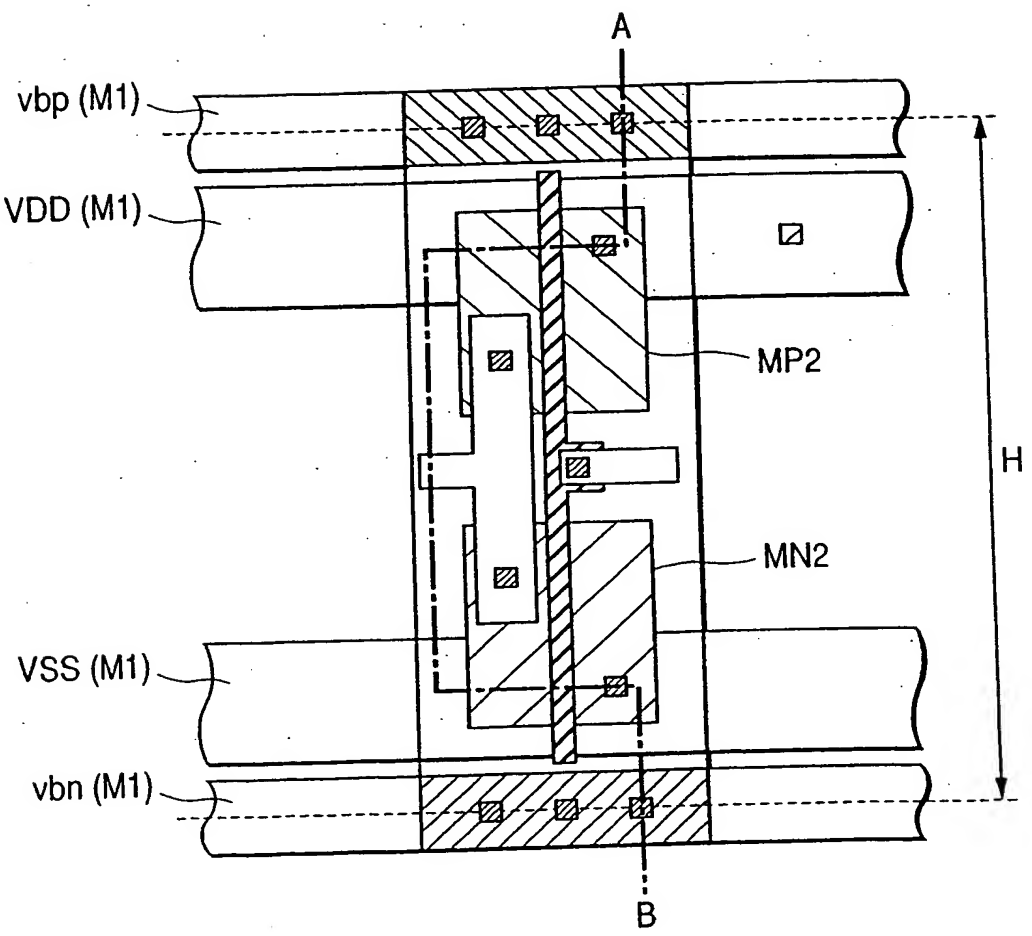
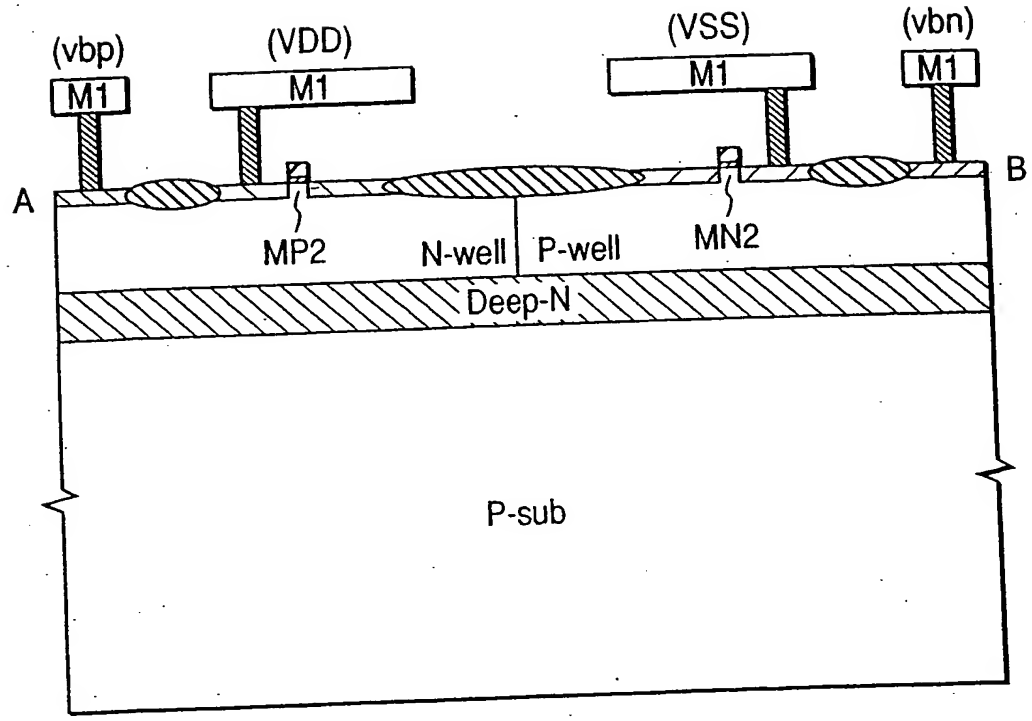

A
vbp (M1)
VDD (M1)
MP2
H
MN2
VSS (M1)
vbn (M1)
B
GATE ELECTRODE
M1
CONTACT HOLE
NMOS ACTIVE AREA
PMOS ACTIVE AREA
SURFACE HIGH DENSITY N AREA FOR PMOS VBB SUPPLY
SURFACE HIGH DENSITY P AREA FOR NMOS VBB SUPPLY

FIG. 18



GATE OXIDIZATION FILM

GATE ELECTRODE

ISOLATION

M1-M2 VIA HOLE

NMOS ACTIVE AREA (N+)

PMOS ACTIVE AREA (P+)

SURFACE HIGH DENSITY N AREA FOR PMOS V_{BB} SUPPLY

SURFACE HIGH DENSITY P AREA FOR NMOS V_{BB} SUPPLY

FIG. 19

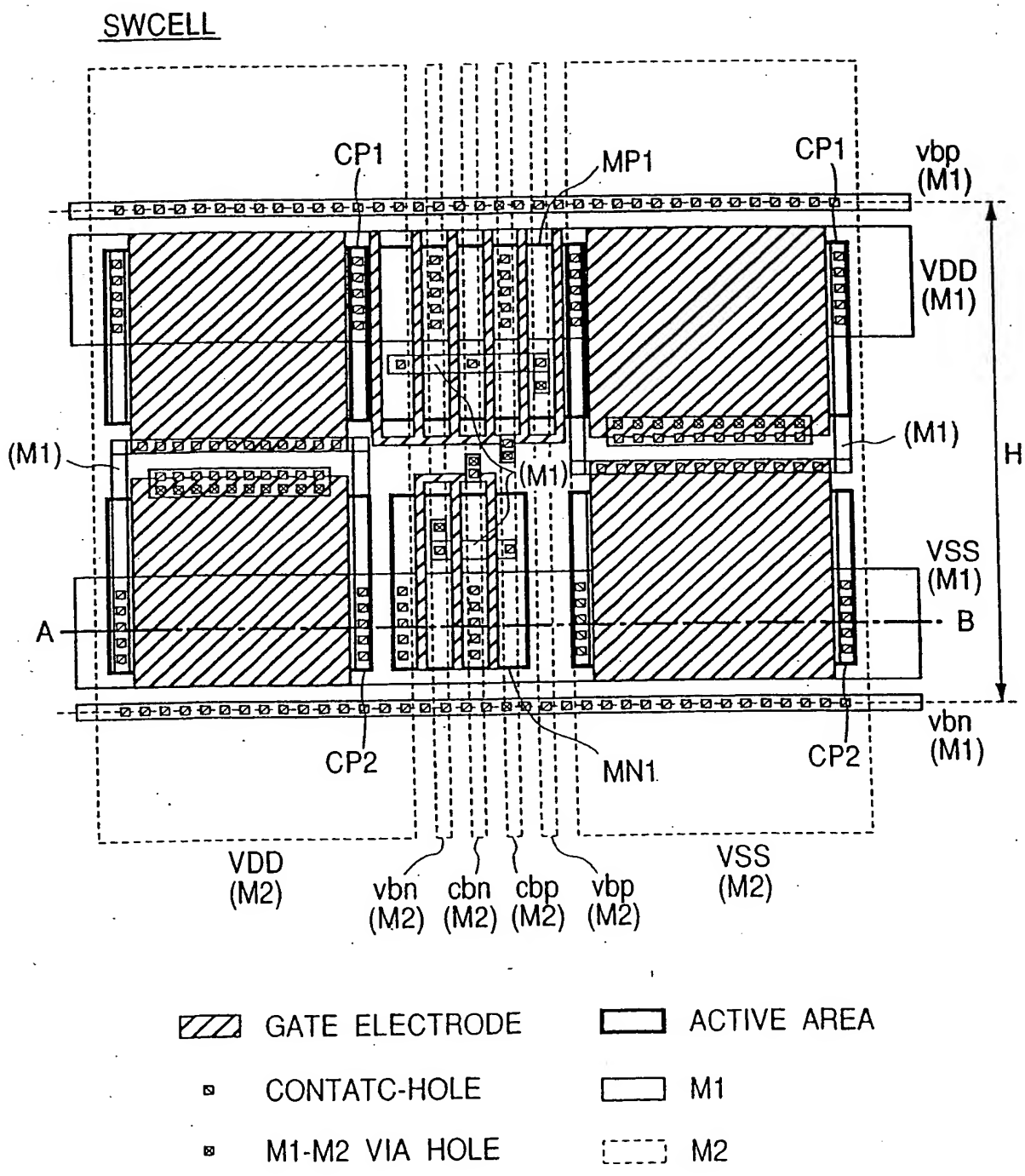

SWCELL
CP1
MP1
CP1
vbp
(M1)
VDD
(M1)
(M1)
(M1)
(M1)
H
VSS
(M1)
A
B
vbn
(M1)
CP2
MN1
CP2
VDD
(M2)
vbn
(M2)
cbn
(M2)
cbp
(M2)
vbp
(M2)
VSS
(M2)
GATE ELECTRODE
ACTIVE AREA
CONTATC-HOLE
M1
M1-M2 VIA HOLE
M2

FIG. 20

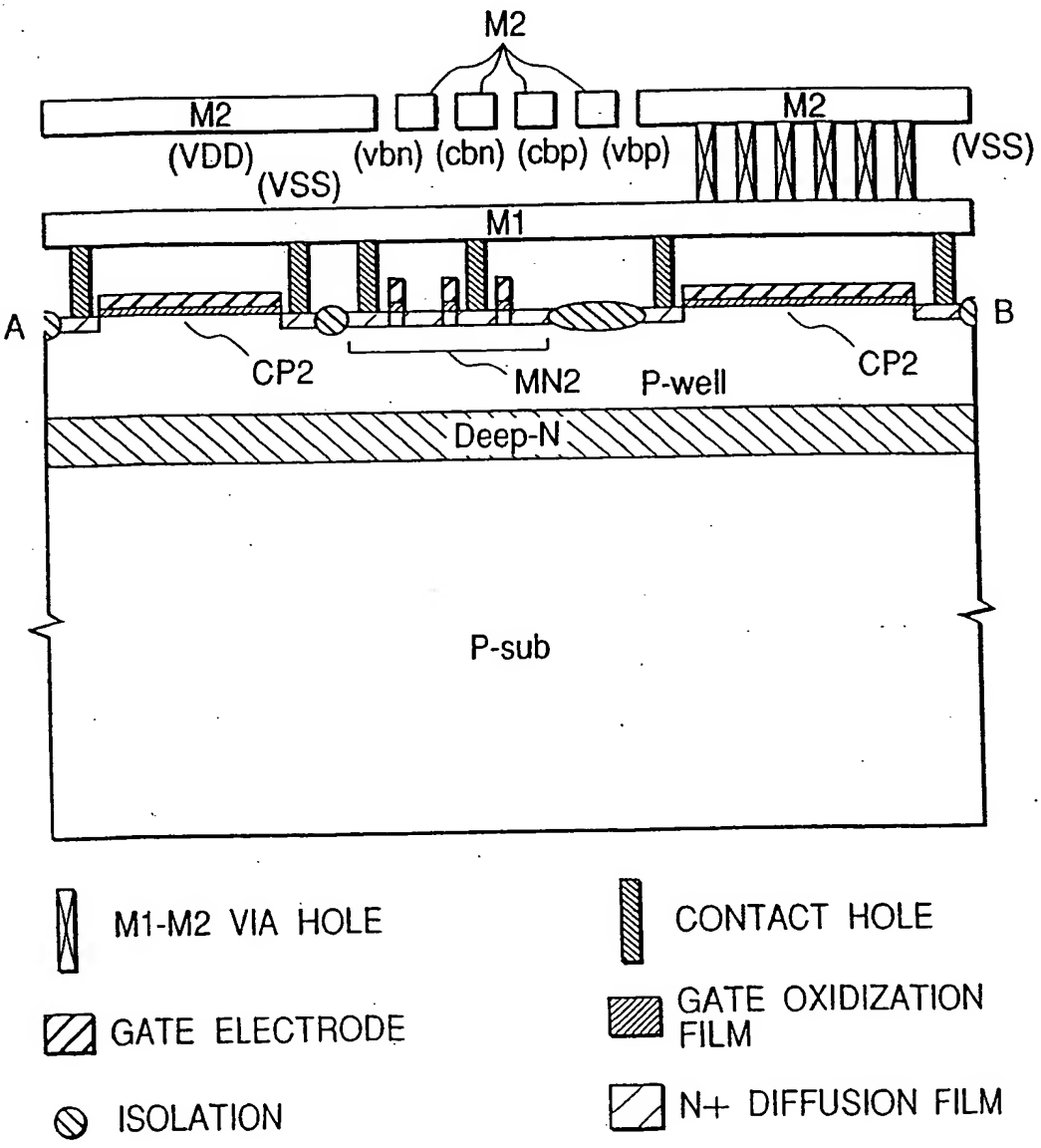

M2
M2
M2
(VDD)
(VSS)
(vbn)
(cbn)
(cbp)
(vbp)
(VSS)
M1
A
B
CP2
MN2
P-well
CP2
Deep-N
P-sub
M1-M2 VIA HOLE
CONTACT HOLE
GATE ELECTRODE
GATE OXIDIZATION FILM
ISOLATION
N+ DIFFUSION FILM

FIG. 21

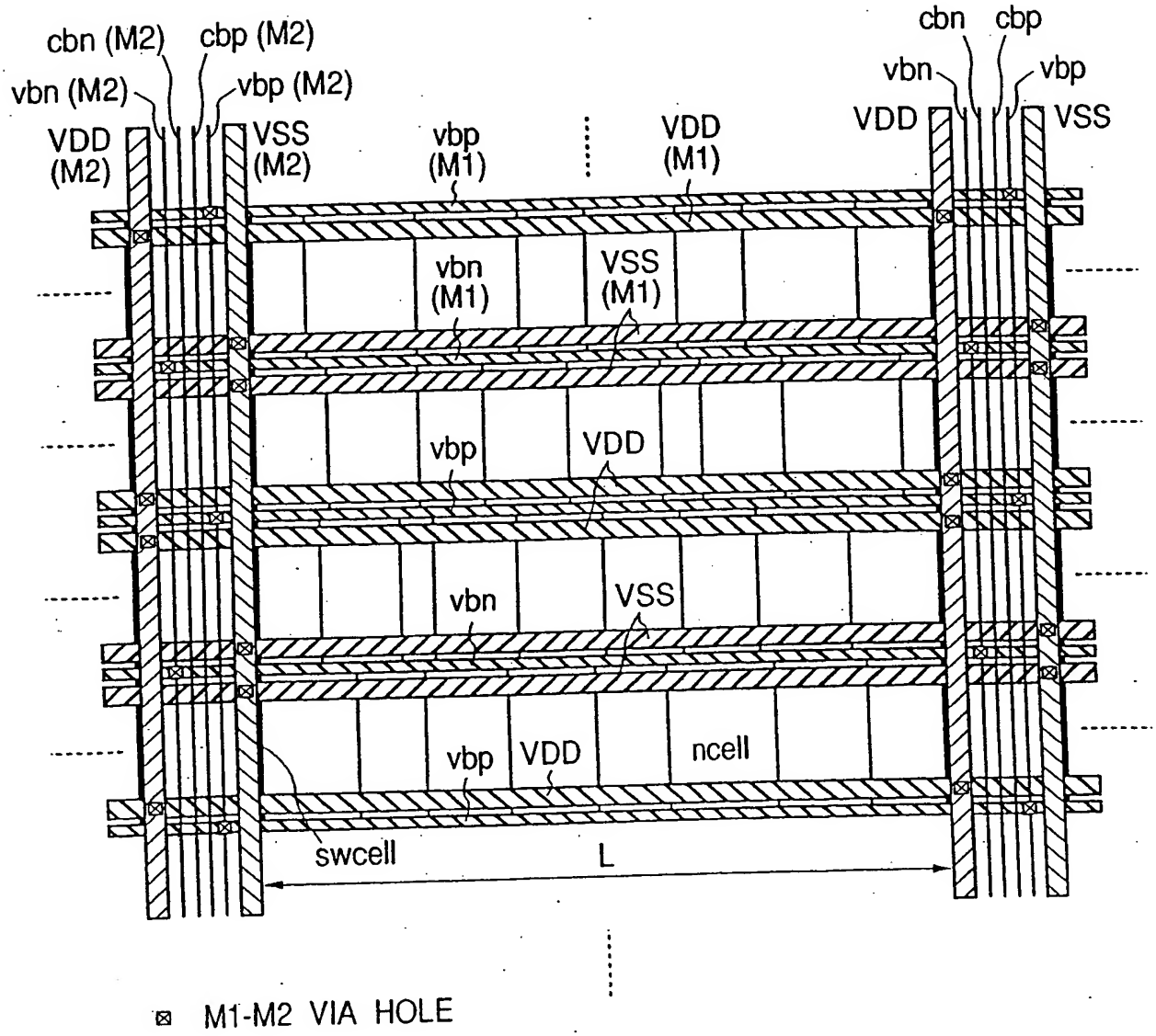

cbn (M2)
cbp (M2)
vbn (M2)
vbp (M2)
VDD (M2)
VSS (M2)
vbp (M1)
VDD (M1)
cbn
cbp
vbn
vbp
VDD
VSS
vbn (M1)
VSS (M1)
vbp
VDD
vbn
VSS
vbp
VDD
ncell
swcell
L
⊠ M1-M2 VIA HOLE

FIG. 22

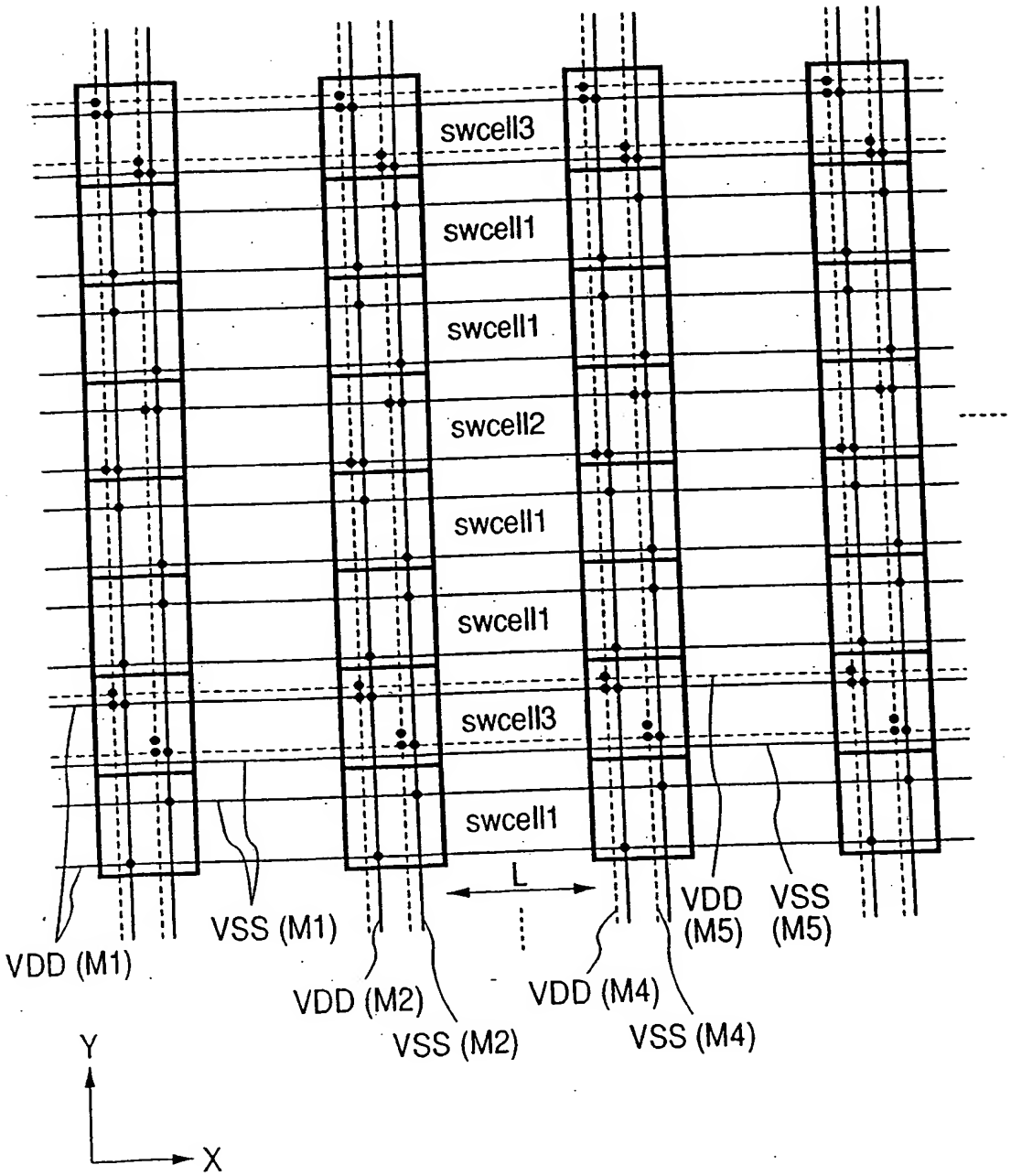

swcell3
swcell1
swcell1
swcell2
swcell1
swcell1
swcell3
swcell1
L
VDD (M1)
VSS (M1)
VDD (M2)
VSS (M2)
VDD (M4)
VSS (M4)
VDD (M5)
VSS (M5)
Y
X

FIG. 23

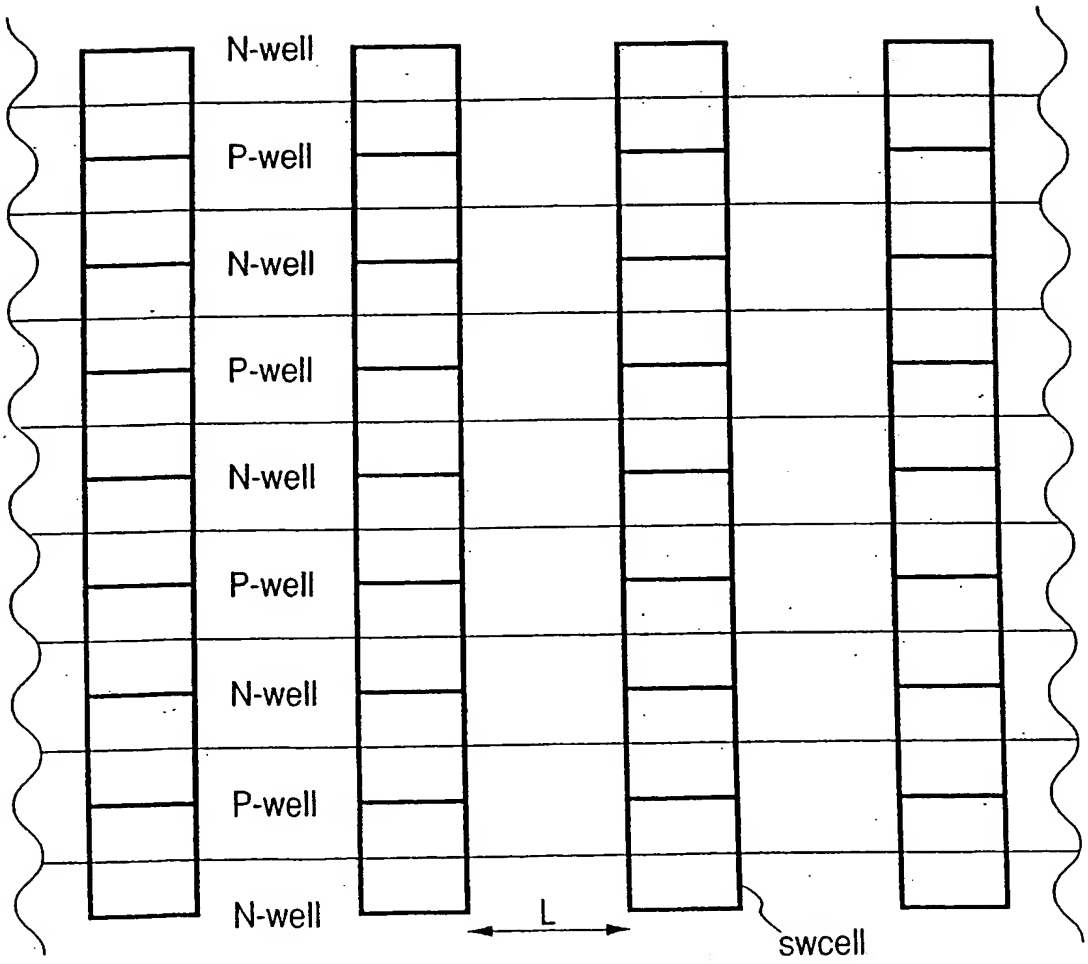

N-well
P-well
N-well
P-well
N-well
P-well
N-well
P-well
N-well
L
swcell

FIG. 24

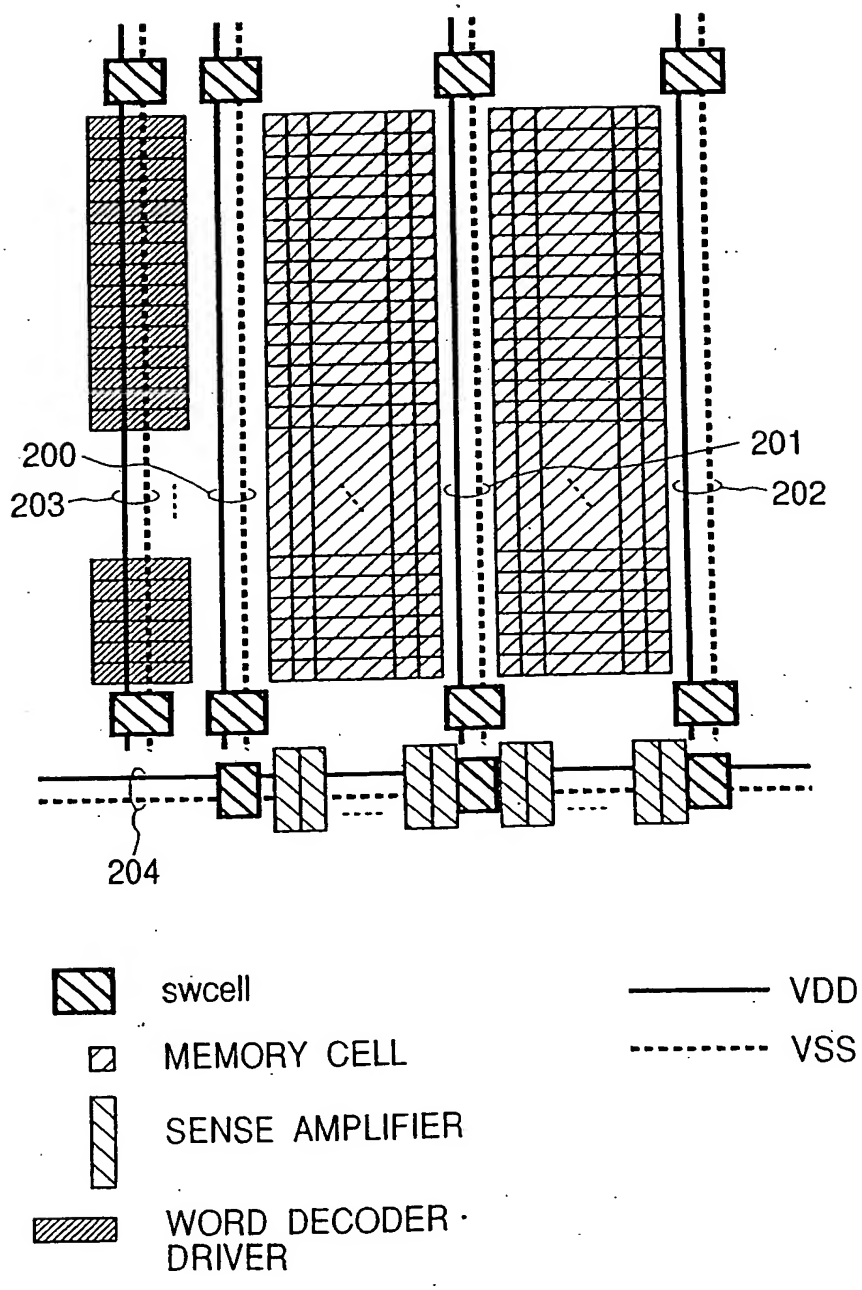

200
203
201
202
204
swcell
MEMORY CELL
SENSE AMPLIFIER
WORD DECODER · DRIVER
VDD
VSS

FIG. 25

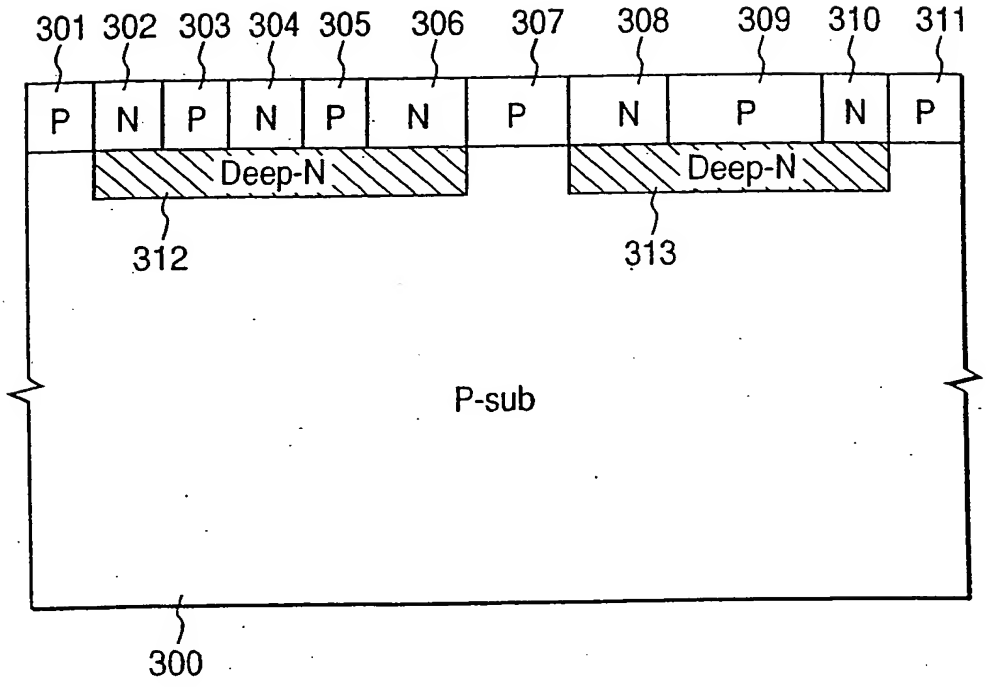

301
302
303
304
305
306
307
308
309
310
311
P
N
P
N
P
N
P
N
P
N
P
Deep-N
Deep-N
312
313
P-sub
300

FIG. 26

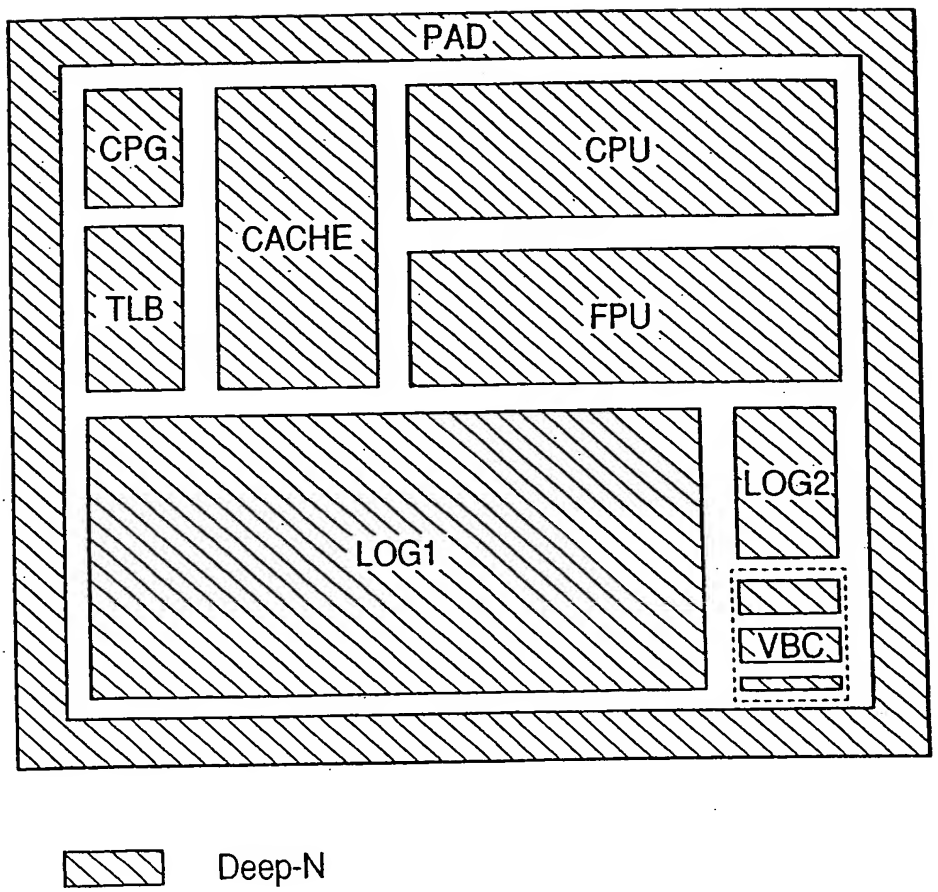


FIG. 27

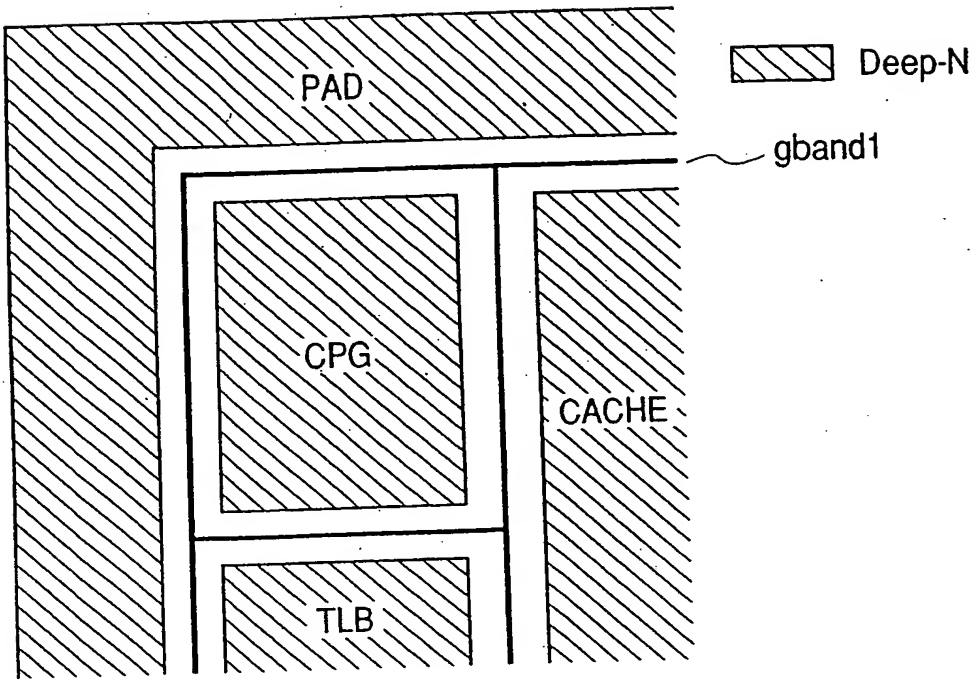

PAD
Deep-N
gband1
CPG
CACHE
TLB

FIG. 28

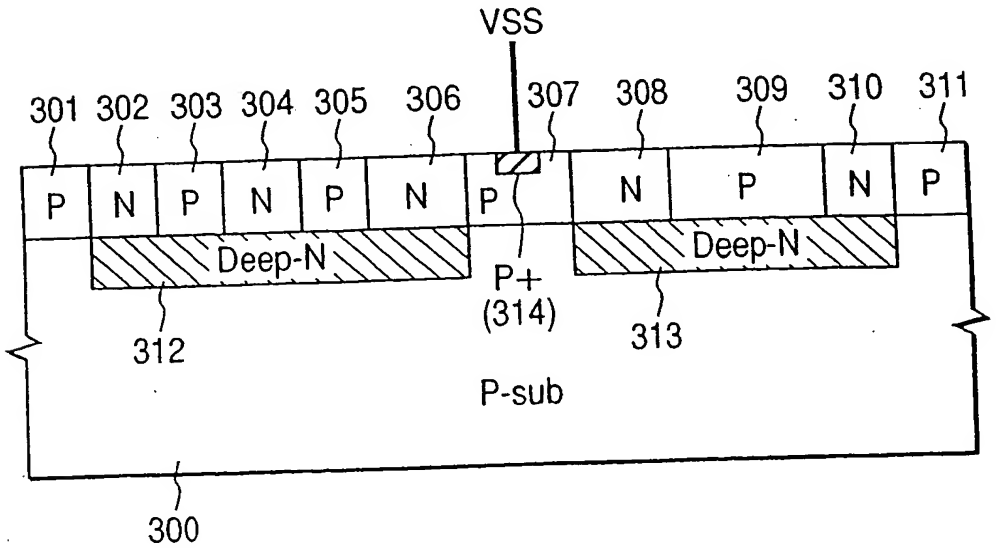

VSS
301
302
303
304
305
306
307
308
309
310
311
P
N
P
N
P
N
P
N
P
N
P
Deep-N
Deep-N
P+
(314)
312
313
P-sub
300

FIG. 29